Vivado Simulator 2017.4

Copyright 1986-1999, 2001-2016 Xilinx, Inc. All Rights Reserved.

Running: C:/Xilinx/Vivado/2017.4/bin/unwrapped/win64.o/xelab.exe -wto e29592b29a394e0580c318f5da7dfa7a --incr --debug typical --relax --mt 2 -L xil\_defaultlib -L secureip --snapshot tb\_State\_Machine\_behav xil\_defaultlib.tb\_State\_Machine -log elaborate.log

Using 2 slave threads.

Starting static elaboration

Completed static elaboration

Starting simulation data flow analysis

Completed simulation data flow analysis

Time Resolution for simulation is 1ps

Compiling package std.standard

Compiling package std.textio

Compiling package ieee.std\_logic\_1164

Compiling package ieee.std\_logic\_arith

Compiling package ieee.std\_logic\_unsigned

Compiling package ieee.numeric\_std

Compiling architecture behavioral of entity xil\_defaultlib.State\_Machine [state\_machine\_default]

Compiling architecture behavioral of entity xil\_defaultlib.tb\_state\_machine

Built simulation snapshot tb\_State\_Machine\_behav